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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,946	10/15/2001	Sergio Morini	IR-2095	9611

2352 7590 04/15/2004

OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY 100368403

EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,946	MORINI ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-21* is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/23/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Response filed March 15, 2004.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuroda (US 5,742,183).

Regarding claim 1, in figures 3A and 4A, Kuroda teaches a digital level shift circuit comprising:

a level shifting device (MN1) that is turned on to make an output transition (col. 5, lines 12-40); and

feedback circuitry (MN2, MP2) that obtains a feedback signal indicating that the level shifting device has made the output transition and that turns off the level shifting device in response to the feedback signal (col. 5, lines 41-54).

Regarding claim 2, in figures 3A and 4A, Kuroda teaches that the level shifting device (MN1) receives a turn-on signal (when n4=VDDH) that turns on the device to make the output transition.

Regarding claim 3, in figures 3A and 4A, Kuroda teaches that the output signal voltage range (does not necessarily mean minimum logic LOW to maximum logic HIGH voltage) extends from an offset voltage (VDDH-VDDL) to an upper voltage (VDDH) that is the sum of the offset voltage (VDDH-VDDL) and a fixed supply voltage (VDDH); and the offset voltage changing rapidly (more rapid than any slower changing voltage).

Regarding claim 4, in figures 3A and 4A, Kuroda teaches that the feedback circuitry includes a feedback device (either MN2/MP2 or MP1), the feedback device providing the feedback signal by turning on (either MN2 or MP1) when the level shifting device makes the output transition.

Regarding claim 5, in figures 3A and 4A, Kuroda teaches that one of the level shifting device (MN1) and the feedback device (either MP2 or MP1) is an n-channel device and the other is a p-channel device (col. 4, lines 62+).

Regarding claim 6, in figures 3A and 4A, Kuroda teaches that the n-channel and p-channel devices are high voltage MOS transistors (higher than any other lower voltage MOS transistors).

Allowable Subject Matter

Claims 7-21 are allowed.

Response to Arguments

Applicant's arguments filed January 23, 2004 have been fully considered but they are not persuasive.

Applicant argues on page 6 of the argument filed January 23, 2004, that "after transistor M_{N1} is turned on (to make the output transition) by an H level signal at terminal S1, transistor M_{N2} is turned on and transistors M_{P1} and M_{P2} are turned off. This, in turn, keeps the gate of level shifting transistor M_{N1} high, and the transistor stays on. Thus, claim 1, which calls for

. . . feedback circuitry that obtains a feedback signal indicating that the level shifting device has made the output transition and that turns off the level shifting device in response to the feedback signal.

is not anticipated by the embodiment shown in Fig. 3A of reference."

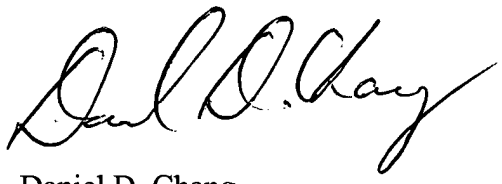
However, when signal at S1 goes from High (1) to Low (0), the level shifting transistor M_{N1} will turn off (see col. 5, lines 41-54). Therefore, "feedback circuitry (MN2, MP2) ... turns off the level shifting device (M_{N1}) in response to the feedback signal.", as set forth in Claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

DC

DANIEL CHANG
PRIMARY EXAMINER